UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,346	09/12/2000	William Lewis Betts	61607-1280	6191

24504 7590 03/19/2004

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
100 GALLERIA PARKWAY, NW
STE 1750
ATLANTA, GA 30339-5948

EXAMINER	
ODOM, CURTIS B	

ART UNIT	PAPER NUMBER
2634	3

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/660,346	BETTS ET AL.	
	Examiner	Art Unit	
	Curtis B. Odom	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18* is/are allowed.

6)☒ Claim(s) *1-14, 19, 21, and 22* is/are rejected.

7)☐ Claim(s) *15-17,20,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: On page 8, line 15, the phrase "constellation vector 27" is suggested to be changed to "eq_xeye 27". Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-14, 19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being obvious over Koslov (U. S. Patent No. 5, 471, 508).

Regarding claim 1, Koslov disclcoses a system (Fig. 2) to derive symbol timing for a receiver, comprising:

a slicer (Fig. 2, block 220, column 11, lines 23-48) that decodes a received signal segment into a discrete data symbol;

a caluculator (Fig. 2, blocks 230 and 250, column 11, lines 23-48) that receives the received signal segment and the discrete data symbol, that derives a timing phase error based upon the received signal segment and discrete data symbol, and computes an average (phase integrator) based upon the timing phase error; and

an oscillator that receives a control signal and that generates symbol timing for a receiver (Fig. 2, block 260), wherein the can be implemented as a numerically controlled oscillator (column 2, lines 15-39).

Koslov does not disclose a circuit that receives the average and that develops a control signal based upon the average.

However, Koslov does disclose an analog loop filter (column 9, lines 24-52) which provides a control signal to an oscillator based upon a phase error signal. Koslov also discloses a digital equivalent of the filter (Fig. 2, block 240, column 11, line 54-column 12, line 9) which also filters a phase error signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the digital loop filter after the phase integrator in order to apply a filtered control signal to the ROM (numerically controlled oscillator) which would allow proper synchronization at the receiver.

Regarding claim 2, which inherits the limitations of claim 1, Koslov discloses the calculator comprises a multiplier (Fig. 2, block 233) and a leaky integrator (Fig. 2, block 250, column 11, lines 48-53).

Regarding claim 3, which inherits the limitations of claim 1, Koslov discloses the slicer employs an advanced data recovery technique for decoding the received signal segment (column 11, lines 29-44).

Regarding claim 4, which inherits the limitations of claim 1, Koslov discloses the circuit comprises a phase locked loop (column 10, lines 61-64).

Regarding claim 5, which inherits the limitations of claim 1, Koslov does not disclose the oscillator is a voltage controlled oscillator. However, Koslov does disclose a voltage controlled oscillator which can be used to symbol timing in the receiver (Fig. 1A, block 80, column 9, lines 41-53). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the VCO as taught by Koslov to allow synchronization in the receiver by generating efficient symbol timing which would properly reproduce the incoming signal at the receiver.

Regarding claim 6, which inherits the limitations of claim 1, Koslov does not disclose the oscillator is configured to generate symbol timing for a transmitter. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the oscillator as taught by Koslov (Fig. 1A, block 80, column 9, lines 41-53) could have been implemented into the transmitter in the same manner in which it was implemented into the receiver to produce symbol timing in the transmitter. Thus, claim 6, does not constitute patentability.

Regarding claim 7, which inherits the limitations of claim 1, Koslov does not disclose the system is part of a point-to-point system. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the system could have been implemented into a point-to-point system to generate symbol timing for recovering transmitted signal. Thus, implementing the system of Koslov into a point-to-point system is deemed a design choice and does not constitute patentability.

Regarding claim 8, which inherits the limitations of claim 7, Koslov does not disclose the system is part of a full duplex system. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the system could have been implemented into a full duplex system to generate symbol timing for recovering transmitted signal. Thus, implementing the system of Koslov into a full duplex system is deemed a design choice and does not constitute patentability.

Regarding claim 9, which inherits the limitations of claim 7, Koslov does not disclose the system is part of a half duplex system. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the system could have been implemented into a half duplex system to generate symbol timing for recovering transmitted signal. Thus, implementing the system of Koslov into a half duplex system is deemed a design choice and does not constitute patentability.

Regarding claims 10-13 which inherit the limitations of claim 1, Koslov does not disclose the system is part of a multi-point system or that the multi-point system can operate on the following protocols: discrete multi-tone, carrier amplitude modulation, or multiple virtual lines. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the system could have been implemented into a multi-point system to generate symbol timing for recovering transmitted signal. The type of protocol used would depend on the design specifications of the device. Thus, implementing the system of Koslov into a multi-point system and choosing an operation protocol is deemed a design choice and does not constitute patentability.

Regarding claim 14, which inherits the limitations of claim 13, Koslov discloses an equalizer in the system (column 11, lines 6-8). Koslov does not disclose the equalizer is a fractionally spaced equalizer producing a plurality of coefficients. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that a fractionally spaced equalizer could have been implemented as the equalized to remove such interference as ISI from the received symbols. Thus, implementing a fractionally spaced equalized is deemed a design choice and does not constitute patentability.

Regarding claim 19, the claimed apparatus includes features corresponding to subject matter mentioned in the above rejection of claim 1, which is applicable hereto.

Regarding claim 21, Koslov discloses a method for deriving symbol timing, comprising the steps:

decoding (Fig. 2, block 220, column 11, lines 23-48) a received signal segment into a discrete data symbol;

calculating (Fig. 2, blocks 230 and 250, column 11, lines 23-48) a timing phase error and an average timing phase error (phase integrator) based upon the received signal segment and discrete data symbol; and

generating symbol timing for a receiver (Fig. 2, block 260) based upon a control signal, wherein the can be implemented as a numerically controlled oscillator (column 2, lines 15-39).

Koslov does not disclose creating a control signal based upon the average timing phase error.

However, Koslov does disclose an analog loop filter (column 9, lines 24-52) which provides a control signal to an oscillator based upon a phase error signal. Koslov also discloses a

digital equivalent of the filter (Fig. 2, block 240, column 11, line 54-column 12, line 9) which also filters a phase error signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the digital loop filter after the phase integrator in order to apply a filtered control signal based upon the average phase error signald to the ROM (numerically controlled oscillator) which would allow proper synchronization at the receiver.

Regarding claim 22, which inherits the limitations of claim 21, Koslov does not disclose generating symbol timing for a transmitter based on the control signal. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the oscillator signal as taught by Koslov (column 2, lines 15-39) could have been transmitted to the transmitter from the received to produce symbol timing in the transmitter. Thus, claim 22, does not constitute patentability.

Allowable Subject Matter

4. Claim 18 is allowable over prior art because related references do not disclose a system to track symbol timing for a receiver including a centroid error calculator and a leaky integrator for receiving timing phase error and the centroid error calculation and for producing an average timing phase error based upon the timing phase error and the centroid error calculation.

5. Claims 15-17, 20, 23, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 703-305-4097. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Curtis Odom
March 15, 2004

STEPHEN CHIN
SUPERVISORY PATENT EXAMINE
TECHNOLOGY CENTER 2600